12-Bit, 20/40/65 MSPS 3 V Low Power A/D Converter

Preliminary Technical Data **AD9237**

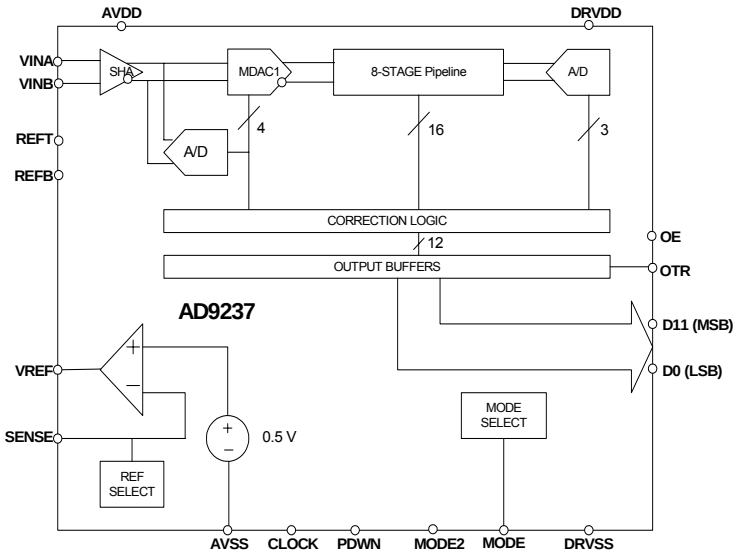
FEATURES

Ultra Low Power
90mW @ 20MSPS;
135mW @ 40MSPS;
190mW @ 65MSPS
SNR = 66.5 dBc (to Nyquist);
SFDR = 82 dBc @ 2.4MHz Analog Input
ENOB = 10.5 bits
DNL=± 0.5 LSB
Differential Input with 500MHz Full Power Bandwidth
Flexible and Selectable Analog Input: 4Vp-p to 1Vp-p
Data Formats Supported; Offset Binary, Twos Complement and Gray Code
Output Enable Pin
2-step power down; Full Power down and Sleep mode

APPLICATIONS

Ultrasound and Medical Imaging
Battery Powered Instruments; Hand-Held Scopemeters; Low Cost Digital Oscilloscopes; Low Power Digital Still Cameras and Copiers; Low power communications

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9237 is a monolithic, single 3V supply, 12-bit, 20/40/65MSPS Analog to Digital Converter with a high performance sample-and-hold amplifier and voltage reference. The AD9237 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20/40/65MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows for a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. With significant power savings over previously available analog to digital converters, the AD9237 is suitable for applications imaging and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary, twos complement, or gray code formats. An out-of-range (OTR) signal indicates an overflow condition, which can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9237 is available in a 32-pin chip scale package and is specified over the industrial temperature range (-40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Operating at 65MSPS, the AD9237 consumes a low 190mW and only consumes 135mW at 40 MSPS and 90mW at 20MSPS.
2. The AD9237 operates from a single 3V power supply, and features a separate digital output driver supply to accommodate 2.5V and 3.3V logic families.
3. The patented SHA input maintains excellent performance for input frequencies beyond Nyquist, and can be configured for single-ended or differential operation.
4. The AD9237 is pin compatible to the AD9235, a 12-bit, 20/40/65 MSPS A/D converter. This allows a simplified path for low power 12-bit systems.
5. The AD9237 is optimized for selectable and flexible input ranges from 4Vp-p to 1Vp-p.
6. Output Enable pin to allow for multiplexing of the outputs.
7. Two-step power down supports a standby mode in addition to a power down mode.
8. The OTR output bit indicates when the signal is beyond the selected input range.

REV PrF 5/18/2005

One Technology Way, P.O Box 9106, Norwood, MA 02062–9106, U.S.A.
Tel: 617/329–4700 **World Wide Web Site: http://www.analog.com**
Fax: 617–326–8703

DC SPECIFICATIONS (AVDD = +3V, DRVDD = +3V, 2Vp-p Input, –0.5dBFS, 1.0V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Temp	Test Level	AD9237BCPZ-20			AD9237BCPZ-40			AD9237BCPZ-65			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	Full	VI	12			12			12			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	12			12			12			Bits
Offset Error	Full	VI		±0.5			±0.5			±0.5		%FSR
Gain Error[1]	Full	VI		±0.5			±0.5			±0.5		%FSR
Differential Nonlinearity (DNL)	Full	IV		±0.5			±0.5			±0.5		LSB
	25°C	I		±0.5			±0.5			±0.5		LSB
Integral Nonlinearity (INL)	Full	IV		±1.2			±1.2			±1.2		LSB
	25°C	I		±1.2			±1.2			±1.2		LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±2			±2			±2		ppm/°C
Gain Error[1]	Full	V		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±5			±5			±5		mV
Load Regulation @ 1.0 mA	Full	V		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
VREF = 0.5 V	25°C	V		1.36			1.36			1.36		LSB rms
VREF = 1.0 V	25°C	V		0.68			0.68			0.68		LSB rms
ANALOG INPUT												
Input Span, VREF = 0.5V; MODE 2 = 0V;	Full	IV			1			1			1	Vp-p
Input Span, VREF = 1.0V; MODE 2 = 0V;	Full	IV			2			2			2	Vp-p
Input Span, VREF = 0.5V; MODE2= AVDD;	Full	IV			2			2			2	Vp-p
Input Span, VREF = 1.0V;MODE2 = AVDD;	Full	IV			4			4			4	Vp-p
Input Capacitance[3]	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	3.0	3.6	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current												
IAVDD[2]	Full	VI		30			44			63		mA
IDRVDD[2]	Full	VI		2			5			7		mA
PSRR	Full	VI		±0.01			±0.01			±0.01		%FSR
POWER CONSUMPTION												
DC Input[4]	Full	V		90			134			188		mW
Sine Wave Input[2]	Full	VI		95			152			216		mW
Power Down Mode[5]	Full	V		1			1			1		mW
Standby Power[6]	Full	V		17			17			17		mW

NOTES
1. Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0V external reference).
2. Measured at maximum Clock Rate, F_{IN} = 2.4MHz, full-scale sine wave, with approximately 5pF loading on each output bit.
3. Input Capacitance refers to the effective capacitance between one differential input pin and AGND.
4. Measured with dc input at Maximum Clock Rate.
5. Power Down Mode power is measured with a dc input, the CLK pin inactive (i.e., set to AVDD or AGND)
6. Standby Mode power is measured with a dc input, the CLK pin active.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

Parameter	Temp	Test Level	AD9237BCPZ-20			AD9237BCPZ-40			AD9237BCPZ-65			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LOGIC INPUTS												
High-Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low-Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High-Level Input Current	Full	IV	-10		10	-10		10	-10		10	µA
Low-Level Input Current	Full	IV	-10		10	-10		10	-10		10	µA
Input Capacitance	Full	V		2			2			2		PF
LOGIC OUTPUTS[1]												
DRVDD = 3.3V												
High-Level Output Voltage (IOH=50µA)	Full	IV	3.29			3.29			3.29			V
High-Level Output Voltage (IOH=0.5mA)	Full	IV	3.25			3.25			3.25			V
Low-Level Output Voltage (IOL=1.6mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL=50µA)	Full	IV			0.05			0.05			0.05	V
DRVDD = 2.5V												
High-Level Output Voltage (IOH=50µA)	Full	IV	2.49			2.49			2.49			V
High-Level Output Voltage (IOH=0.5mA)	Full	IV	2.45			2.45			2.45			V
Low-Level Output Voltage (IOL=1.6mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL=50µA)	Full	IV			0.05			0.05			0.05	V

NOTES:
1. Output Voltage Levels measured with 5pF load on each output.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

Parameter	Temp	Test Level	AD9237BCPZ-20			AD9237BCPZ-40			AD9237BCPZ-65			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CLOCK INPUT PARAMETERS												
Max Conversion Rate	Full	IV	20			40			65			MSPS
Min Conversion Rate	Full	V			1			1			1	MSPS
CLOCK PERIOD	Full	V	50.0			25.0			16.6			ns
CLOCK Pulsewidth High	Full	V	15			8.8			6.8			ns
CLOCK Pulsewidth Low	Full	V	15			8.8			6.8			
DATA OUTPUT PARAMETERS												
Output Delay[1] (t_{OD})	Full	V		3.5			3.5			3.5		ns
Pipeline Delay (Latency)	Full	V		9			9			9		Cycles
Output Enable Time	Full	V		6			6			6		ns
Output Disable Time	Full	V		3			3			3		ns
Aperture Delay	Full	V		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter)	Full	V		0.5			0.5			0.5		ps rms
Wake-Up time[2] (Sleep Mode)	Full	V		2.5			2.5			2.5		ms
Wake-Up time (Standby Mode)	Full	V		tbd			tbd			tbd		ns
OUT-OF_RANGE RECOVERY TIME	Full	V		1			1			2		cycles

NOTES:
1. Valid Data Delay is measured from CLOCK 50% transition to DATA 50% transition, with 5pF load.
2. Wake-Up Time is dependant on value of decoupling capacitors, typical values shown with 0.1µF and 10µF capacitors on REFT and REFB.
Specifications subject to change without notice.

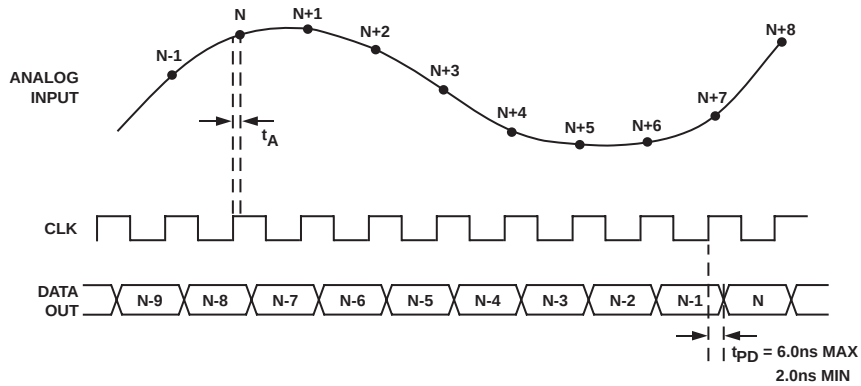


Figure 1. Timing Diagram

AC SPECIFICATIONS (AVDD = +3V, DRVDD = +3V, 2Vp-p Input, –0.5dBFS, 1.0V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Temp	Test Level	AD9237BCPZ-20			AD9237BCPZ-40			AD9237BCPZ-65			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE RATIO												
F_{INPUT} = 2.4 MHz	Full	IV		66.5			66.5			66.5		dB
	25°C	I		66.5			66.5			66.5		dB
F_{INPUT} = 10.3 MHz	Full	IV		66.5								dB
	25°C	I		66.5								dB
F_{INPUT} = 19.6 MHz	Full	IV					66.5					dB
	25°C	I					66.5					dB
F_{INPUT} = 30 MHz	Full	IV								66.5		dB
	25°C	I								66.5		dB
F_{INPUT} = 70 MHz	25°C	V		tbd			tbd			tbd		dB
SIGNAL-TO-NOISE RATIO AND DISTORTION												
F_{INPUT} = 2.4 MHz	Full	IV		65			65			65		dB
	25°C	I		65			65			65		
F_{INPUT} = 10.3 MHz	Full	IV		65								dB
	25°C	I		65								dB
F_{INPUT} = 19.6 MHz	Full	IV					65					dB
	25°C	I					65					dB
F_{INPUT} = 30 MHz	Full	IV								65		dB
	25°C	I								65		dB
F_{INPUT} = 70 MHz	25°C	V		tbd			tbd			tbd		dB
EFFECTIVE NUMBER OF BITS												
F_{INPUT} = 2.4 MHz	25°C	V		10.5			10.5			10.5		Bits
F_{INPUT} = 10.3 MHz	25°C	V		10.5								Bits
F_{INPUT} = 19.6 MHz	25°C	V					10.5					Bits
F_{INPUT} = 30 MHz	25°C	V								10.5		Bits
F_{INPUT} = 70 MHz	25°C	V		tbd			tbd			tbd		Bits
TOTAL HARMONIC DISTORTION												
F_{INPUT} = 2.4 MHz	Full	IV		80			80			80		dB
	25°C	I		80			80			80		
F_{INPUT} = 10.3 MHz	Full	IV		80								dB
	25°C	I		80								dB
F_{INPUT} = 19.6 MHz	Full	IV					80					dB
	25°C	I					80					dB
F_{INPUT} = 30 MHz	Full	IV								80		dB
	25°C	I								80		dB
F_{INPUT} = 70 MHz	25°C	V		tbd			tbd			tbd		dB
WORST HARMONIC (2^{nd} or 3^{rd})												
F_{INPUT} = 9.7 MHz	Full	IV		tbd								dB
F_{INPUT} = 19.6 MHz	Full	IV					tbd					dB
F_{INPUT} = 30 MHz	Full	IV								Tbd		dB
SPURIOUS FREE DYNAMIC RANGE												
F_{INPUT} = 2.4 MHz	Full	IV		82			82			82		dBc
	25°C	I		82			82			82		
F_{INPUT} = 10.3 MHz	Full	IV		82								dBc
	25°C	I		82								dBc
F_{INPUT} = 19.6 MHz	Full	IV					82					dBc
	25°C	I					82					dBc
F_{INPUT} = 30 MHz	Full	IV								82		dBc
	25°C	I								82		dBc
F_{INPUT} = 70 MHz	25°C	V		tbd			tbd			tbd		dBc

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Pin Name	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	-0.3	+3.9	V
DRVDD	DGND	-0.3	+3.9	V
AGND	DGND	-0.3	+0.3	V
AVDD	DRVDD	-3.9	+3.9	V
Digital Outputs	DGND	-0.3V	DRVDD +0.3	V
CLK, OEB	AGND	-0.3V	AVDD +0.3	V
MODE, MODE2	AGND	-0.3V	AVDD +0.3	V
VIN+, VIN-	AGND	-0.3V	AVDD +0.3	V
VREF	AGND	-0.3V	AVDD +0.3	V
SENSE	AGND	-0.3V	AVDD +0.3	V
REFB, REFT	AGND	-0.3V	AVDD +0.3	V
PDWN	AGND	-0.3V	AVDD +0.3	V
ENVIRONMENTAL[2]				
Operating Temperature		-40	85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		–65	150	°C

NOTES

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

[2] Typical thermal impedances (32-terminal LFCSP); θ_{JA} = 32.5°C/W; θ_{JC} = 32.71°C/W. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-1.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9237BCPZ-20[1]	–40°C to +85°C	32-Lead Frame Chip Scale Package (LFCSP)	CP-32
AD9237BCPZ-40	–40°C to +85°C	32-Lead Frame Chip Scale Package (LFCSP)	CP-32
AD9237BCPZ-65	–40°C to +85°C	32-Lead Frame Chip Scale Package (LFCSP)	CP-32
AD9237BCP-20EB		LFCSP Evaluation Board (w/ AD9237BCPZ-20)	
AD9237BCP-40EB		LFCSP Evaluation Board (w/ AD9237BCPZ-40)	
AD9237BCP-65EB		LFCSP Evaluation Board (w/ AD9237BCPZ-65)	

[1] It is recommended that the exposed paddle be soldered to the ground plane. There is an increased reliability of the solder joints, and maximum thermal capability of the package is achieved with the exposed paddle soldered to the customer board.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at TMIN or TMAX.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and can be manifested as noise on the input to the ADC.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD – 1.76)/6.02$$

it is possible to obtain a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

CLOCK PULSEWIDTH AND DUTY CYCLE

Pulsewidth high is the minimum amount of time that the clock pulse should be left in the logic "1" state to achieve rated performance: pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specs define an acceptable clock duty cycle.

MINIMUM CONVERSION RATE

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

MAXIMUM CONVERSION RATE

The clock rate at which parametric testing is performed.

OUTPUT PROPAGATION DELAY

The delay between the clock logic threshold and the time when all bits are within valid logic levels.

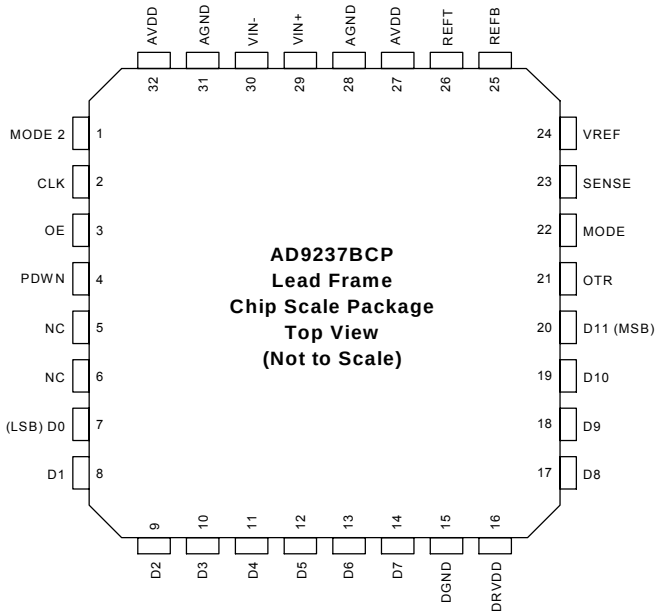
TWO TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

PIN FUNCTION DESCRIPTIONS (32 Pin LFCSP Package)

<table>
<tr><th>Pin No.</th><th>Name</th><th>Function</th></tr>
<tr><td>1</td><td>MODE 2</td><td>SHA Gain Select and Power Control (see Figure 2)
<table>
<tr><th>MODE2 Connection</th><th>SHA Gain</th><th>Auto Power Control</th></tr>
<tr><td>AVDD</td><td>1</td><td>Disabled</td></tr>
<tr><td>2/3 AVDD</td><td>1</td><td>Enabled</td></tr>
<tr><td>1/3 AVDD</td><td>2</td><td>Enabled</td></tr>
<tr><td>AGND</td><td>2</td><td>Disabled</td></tr>
</table></td></tr>
<tr><td>2</td><td>CLK</td><td>Clock Input Pin</td></tr>
<tr><td>3</td><td>OE</td><td>Output Enable Pin (active low)</td></tr>
<tr><td>4</td><td>PDWN</td><td>Power-Down function selection.
<table>
<tr><td>PWDN</td><td>Function</td></tr>
<tr><td>AVDD</td><td>Power Down Mode: All circuits powered down, no clock</td></tr>
<tr><td>1/3 AVDD</td><td>Standby Mode: Only current & voltage references powered up</td></tr>
<tr><td>AGND</td><td>Power Up</td></tr>
</table></td></tr>
<tr><td>5,6</td><td>DNC</td><td>Do Not Connect</td></tr>
<tr><td>7-14, 17-20</td><td>D0 (LSB) – D11 (MSB)</td><td>Data Output Pins</td></tr>
<tr><td>15</td><td>DGND</td><td>Digital ground.</td></tr>
<tr><td>16</td><td>DRVDD</td><td>Digital Output Driver Supply.</td></tr>
<tr><td>21</td><td>OTR</td><td>Out of Range Flag</td></tr>
<tr><td>22</td><td>MODE</td><td>Output Data Format Select and Duty Cycle Stabilizer Control
<table>
<tr><th>MODE Connection</th><th>Output Data Format</th><th>Duty Cycle Stabilizer</th></tr>
<tr><td>AVDD</td><td>Twos Complement</td><td>Disabled</td></tr>
<tr><td>2/3 AVDD</td><td>Twos Complement</td><td>Enabled</td></tr>
<tr><td>1/3 AVDD</td><td>Offset Binary</td><td>Enabled</td></tr>
<tr><td>AGND</td><td>Offset Binary</td><td>Disabled</td></tr>
</table></td></tr>
<tr><td>23</td><td>SENSE</td><td>Reference mode/Input Full Scale Select</td></tr>
<tr><td>24</td><td>VREF</td><td>Voltage Reference Input/Output.</td></tr>
<tr><td>25</td><td>REFB</td><td>Differential Reference (-).</td></tr>
<tr><td>26</td><td>REFT</td><td>Differential Reference (+).</td></tr>
<tr><td>27,32</td><td>AVDD</td><td>Analog Power Supply.</td></tr>
<tr><td>28,31</td><td>AGND</td><td>Analog ground.</td></tr>
<tr><td>29</td><td>VIN+</td><td>Analog Input Pin (+).</td></tr>
<tr><td>30</td><td>VIN-</td><td>Analog Input Pin (-).</td></tr>
</table>

Preliminary LFCSP Pin Configuration



TYPICAL PERFORMANCE CHARACTERISTICS

(AVDD = 3.0 V, DRVDD = 3.0 V, f_{SAMPLE} = 65 MSPS, DCS Disabled, 2 Vp-p Differential Input, A_{IN} = –0.5 dBFS, 1.0 V internal reference, T_A = 25°C, unless otherwise noted.)

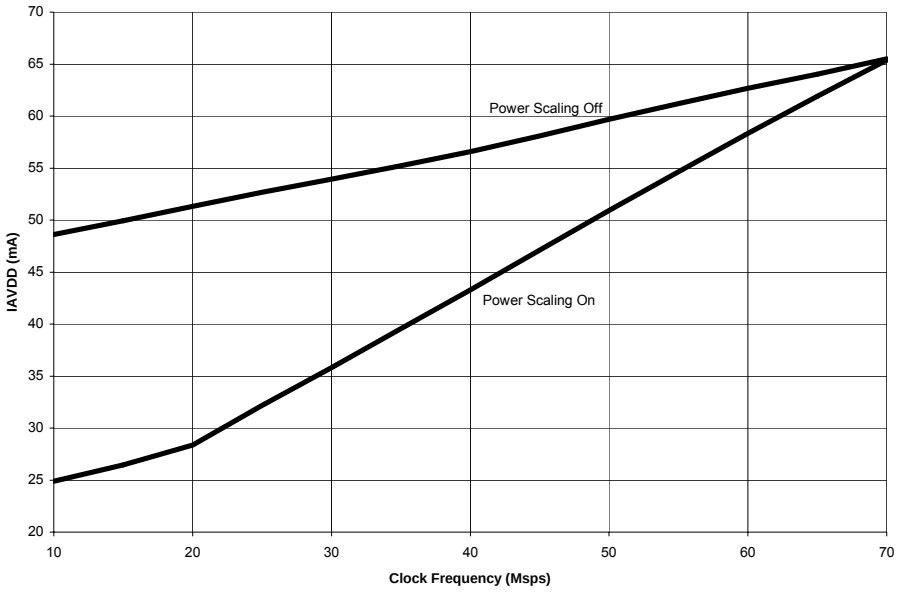
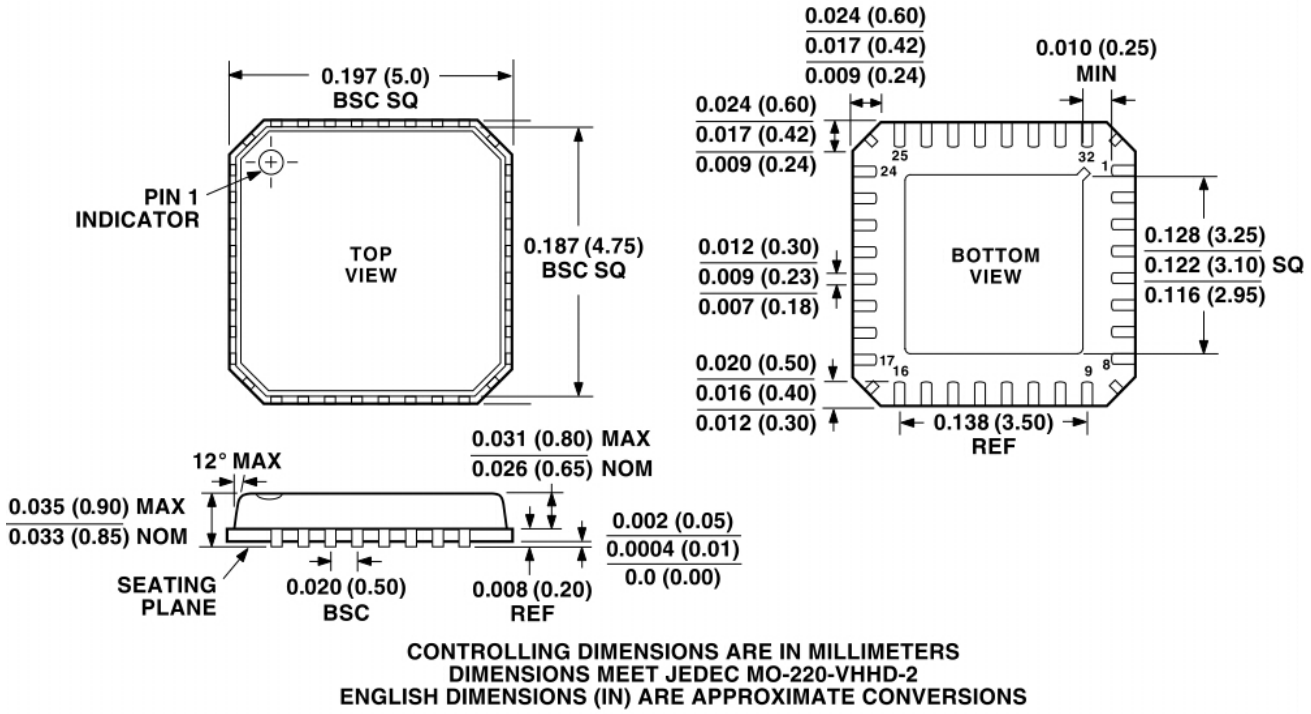


Figure 2. AD9237-65 Analog Current vs. Clock Frequency vs. Power Scaling



32-LFCSP Package Dimensions